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EXAMINER

THAIL

ART UNIT

PAPER NUMBER

2811

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/199,305

Applicant(s)

Ohsawa et al.

Examiner

Luan Thai

Group Art Unit

2811

☒ Responsive to communication(s) filed on Feb 22, 2000☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims☒ Claim(s) 1-15 is/are pending in the application.Of the above, claim(s) 6-10 is/are withdrawn from consideration.☐ Claim(s) _____ is/are allowed.☒ Claim(s) 1-5 and 11-15 is/are rejected.☐ Claim(s) _____ is/are objected to.☐ Claims _____ are subject to restriction or election requirement.**Application Papers**☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.☐ The drawing(s) filed on _____ is/are objected to by the Examiner.☒ The proposed drawing correction, filed on Feb 22, 2000 is ☒ approved ☐ disapproved.☐ The specification is objected to by the Examiner.☐ The oath or declaration is objected to by the Examiner.**Priority under 35 U.S.C. § 119**☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
☐ received.

☐ received in Application No. (Series Code/Serial Number) _____☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).**Attachment(s)**☒ Notice of References Cited, PTO-892☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 11☐ Interview Summary, PTO-413☐ Notice of Draftsperson's Patent Drawing Review, PTO-948☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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DETAILED ACTION

This Office action is responsive to the amendment filed February 22, 2000

Claims **1-13 and 14-15 (newly added claims)** are pending in this application.

Claims **6-10**, directed to the method, were withdrawn from further consideration.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

2. Claims **1-3** are rejected under 35 U.S.C. 102(e) as being anticipated by Chia et al. (5,841,191) as set forth in the previous Office Action paper Number 8 and now repeated.

With respect to claims **1-2**, Chia et al. discloses (see figures 1-2) a semiconductor device comprising: a plurality of wiring films 14' form on a front surface of a base 10' (see figure 2) comprising an insulating tape 10" (figure 2) and having electrode-forming holes 16 (Col. 2, lines 1+), the surfaces of the wiring films 14' and the surface of the base 10' being positioned on the same plane (see figure 2) and a part of the wiring films overlapping with the electrode-forming holes (see figure 2); a conductive material embedded into the electrode-forming holes (Col. 2, lines 6+) to form external electrodes on the back surface, away from the wiring films, of the base; a semiconductor element 20 positioned on the front surface of the base, the back surface of the

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semiconductor element being bonded to the front surface of the base; wires 24 for bonding the electrodes of the semiconductor element to the corresponding wiring films; and a resin sealed the semiconductor element and wires. Although Chia et al. does not specifically disclose the claimed insulating film therebetween the semiconductor element and the base, this feature is seen to be an inherent teaching of that device since a means of mounting the semiconductor element on the top surface of the base is disclosed (Col. 2, lines 63+) and it is apparent that some type of insulating material must be present between the semiconductor element and the base for securing the semiconductor element on the base.

With respect to claim 3, Chia et al. further discloses a metal ring 30 being bonded on the front surface of the base at the exterior of the connecting sections with wires in the wiring films 14' (see figure 2).

3. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Distefano et al. (5,821,608) as set forth in the previous Office Action paper Number 8 and now repeated.

With respect to claims 1-2, Distefano et al. discloses (see figures 3F-3G) a semiconductor device comprising: a plurality of wiring films 50, 55 form on a front surface of a base 30 comprising an insulating tape 30' (see figure 3F-3G) and having electrode-forming holes 40' (see figure 3F), the surfaces of the wiring films 50' and the surface of the base 30' being positioned on the same plane (see figure 3G) and a part of the wiring films overlapping with the electrode-forming holes; a conductive material embedded into the electrode-forming holes 40' (see figure 3F) to form external electrodes on the back surface, away from the wiring films, of the base; a

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semiconductor element 10 positioned on the front surface of the base with an insulating film 80 therebetween, the back surface of the semiconductor element being bonded to the front surface of the base; wires 140 for bonding the electrodes 20 of the semiconductor element to the corresponding wiring films; and a resin 60' sealed the semiconductor element and wires.

With respect to claim 3, Distefano et al. further discloses a metal ring 110 being bonded on the front surface of the base at the exterior of the connecting sections with wires in the wiring films 14' (see figures 2F and 3G).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chia et al. (5,841,191) and/or Distefano et al. (5,821,608) as set forth in the previous Office Action paper Number 8 and now repeated.

With respect to claims 11-12, Chia et al. and/or Distefano et al. disclose all the limitations of the claimed invention as detailed above with the exception of the semiconductor device being comprised of an electronic device. It would have been obvious for the semiconductor device as taught by Chia et al. and/or Distefano et al. to be used as intended in a larger electronic device.

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6. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chia et al. (5,841,191) and/or Distefano et al. (5,821,608) in view of McCormick et al. (5,909,057) as set forth in the previous Office Action paper Number 8 and now repeated.

With respect to claims 4 and 13, Chia et al. and/or Distefano et al. disclose all the limitations of the claimed invention as detailed above with the exception of a reinforcement having a downward indented face covering the semiconductor element.

McCormick et al. while relates to a similar semiconductor device teaches (see figures 2B-2F and 4A-4B) a reinforcement 214 having a downward indented face covering the semiconductor element 200 in order to prevent the semiconductor element from being warping or other wise moving during the curing step (Col. 8, lines 1+).

McCormick et al., Chia et al. and/or Distefano et al. are analogous art because they are from the same field of endeavor, that is the semiconductor art. It would have been obvious to one having ordinary skill in the art to combine the reinforcement as taught by McCormick et al. into Chia et al.'s and/or Distefano et al.'s device in order to prevent the semiconductor element from being warping or other wise moving during the curing step.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chia et al. (5,841,191) in view of Shim et al. (5,708,567) as set forth in the previous Office Action paper Number 8 and now repeated.

With respect to claim 5, Chia et al. discloses all the limitations of the claimed invention as detailed above with the exception of the base having vent holes.

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Shim et al. while relates to a similar semiconductor device teaches (see figure 1) the base 20 having the vent holes 23 is well known in the art for the purpose of generating the heat from the semiconductor chip (Col. 1, lines 45+).

Chia et al. and Shim et al. are analogous art because they are from the same field of endeavor, that is the semiconductor art. It would have been obvious to one having ordinary skill in the art to apply the conventional vent holes formed in the base as taught by Shim et al. into Chia et al.'s device for the purpose of generating the heat from the semiconductor chip.

8. Claims **14-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chia et al. (5,841,191) and/or Distefano et al. (5,821,608) as applied to claims 11 and 1, respectively, above and further in view of Tagusa et al. (4,963,002).

With respect to claims 14-15, the proposed device of Chia et al. and/or Distefano et al. discloses all the limitations of the claimed invention as detailed above with the exception of a nickel layer covering the copper layer of the wiring film.

Tagusa et al. while relate to a similar semiconductor package design teach a wiring layer being provided with a nickel film layer formed thereon to improve the electrical and mechanical interconnection between the integrated circuit chip and the wiring formed on the base substrate (Col. 2, lines 50+).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Tagusa et al.'s teachings into the proposed device of Chia et al. and/or Distefano et

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al. in order to improve the electrical and machanical interconnection between the integrated circuit chip and the wiring formed on the base substrate.

9. The following references are cited as of interest to this application:

U.S. Patent No. 5,909,085 to Yano is cited for showing the surface of the wiring film and the surface of the base being positioned on the same plane and U.S. Patent No. 5,859,475 to Freyman et al. is cited for showing the metal ring being bonded on the front surface of the base.

Response to Arguments

10. Applicant's arguments with respect to claims 1-5 and 11-13, filed on February 22, 2000 have been fully considered but they are not persuasive. Specifically:

(A) Applicant argues, in page 4, second paragraph, of the Remarks, that the portion that the examiner indicates as insulating base 10" (Chia et al.'s reference) is a solder mask layer 22 and that contact layer 14-16 do not lie in the plane of such insulating base.

In response, the examiner points out that, although Chia et al. do not label the layer 22 as a base, figure 2 of Chia et al. do not distinguish from the claimed structure (as detailed above), and Chia's figure 2 clearly shows that the top surface of the wirings 14-16 lie in the plane of such insulating base 10". Further, the labels nonetheless are meaningless. The Chia's structure anticipates Applicant's claimed structure regardless of whether the layer is labeled "base". See *In re Pearson*, 181 USPQ 642; *Fx parte Minks* 169 USPQ 120; or *In re Swinehart* 169 USPQ 226, all of which make it clear that mere "labels" or "statements of in intended use" as we have here in "base" do not distinguish over Chia's structure which may be likewise labeled.

(B) Applicant argues, in page 5, first paragraph, of the Remarks, that the base 30' (Distefano et al. reference) does not have the semiconductor element mounted thereon.

In response, the examiner confirm that Distefano et al.'s figure 3F discloses the semiconductor element 10 being mounted on the base 30' with an insulating film therebetween (Distefano et al.'s Col. 6, lines 10+).

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(C) Applicant argues, in page 5, second paragraph, of the Remarks, that Shim et al. does not teach or suggest "vent holes" as applicant claimed in claim 5.

In response, the examiner points out that, although Shim et al. does not label the holes vertically formed on the chip mounting portion of the base 20 as that applicant claimed "vent holes", the holes disclosed by Shim et al. are considered as "vent holes" for their function of heat dissipating improvement for the device (Shim et al.'s Col. 1, lines 45+ and Col. 3, lines 56+). Further, figure 2 of Shim et al. does not distinguish from the claimed structure and the labels nonetheless are meaningless. The Shim et al.'s structure anticipates Applicant's claimed structure regardless of whether the layer is labeled "plated through holes". See *In re Pearson*, 181 USPQ 642; *Fx parte Minks* 169 USPQ 120; or *In re Swinehart* 169 USPQ 226, all of which make it clear that mere "labels" or "statements of in intended use" as we have here in "vent holes" do not distinguish over Shim et al.'s structure which may be likewise labeled.

Conclusion

11. Applicant's amendment filed on February 22, 2000 have been fully considered but they are not persuasive. Therefore, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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12. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

13. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to **Luan Thai** whose telephone number is (703) 308-1211. The Examiner is in the Office generally between the hours of 7:30 AM to 4:00 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is (703) 308-0956.

04/12/2000

Luan Thai

Tom Thomas